Defence Science Journal, Vol. 69, No. 3, May 2019, pp. 254-258, DOI : 10.14429/dsj.69.14412

Efficient Digital System Management using IEEE 1451.0 Enabled Control Architecture

J. Kamala*, B. Umamaheswari, and T. Jaibalaganesh

College of Engineering, Guindy, Anna University, Chennai – 600 025, India
**E-mail: jkamalaa@annauniv.edu*

ABSTRACT

The IEEE and National Institute of Standards and Technology have formulated an open universal standard called IEEE 1451 for 'Smart Transducer Interface' with digital systems. The objectives of this paper is to propose IEEE 21450 enabled control architectures for efficient management of power system with embedded system parameters as electronic documentation. The control architecture accommodates appropriate number of transducer interface module along with transducer electronic data sheet, which enables active calibration, adaptive tuning and failure proof operation of system management. Smart controller functionalities are implemented by Artix 7 field programmable gate array (FPGA). Interface requirements, hardware utilisation, timing informations are provided for specific hardware. Calibration of sensor data, estimator execution and IEEE service command for read transducer data are validated through Xilinx simulations.

Keywords: Smart transducer interface; Calibration; Transducer interface module; Transducer electronic data sheet

1. INTRODUCTION

The electrical subsystems of military vehicles are increasing both in quantity and complexity due to increasing level of precision, versatility and operability. More research have been carried to achieve fuel efficiency, better reliability, battery management of common electric vehicles considering all real time constraints[1-9]. Research is not carried out in the field of design of controller for energy management of military vehicles. Specification and design of controllers for military vehicles is different from commercial vehicles. This paper focuses on the design of smart digital controller for military vehicles.

Military vehicles are powered by engine/generator and a battery pack. Loads include traction motors and other electrical loads. Power drawn from the engine and battery is optimised to achieve desired vehicle speed and maintain SOC of battery by the controller. Electrical loads are classified into vital, semi-vital and non-vital loads[10]. All loads are connected to hybrid power source through two bus system with switches. Switch configuration is achieved to maximise power delivered to load. Higher priority is provided to vital loads. An optimal control strategy is developed to minimise fuel consumption, achieve desired velocity profile, power the loads and maintain SoC (state of charge) of battery.

Military vehicle's reliability is improved by controller based on inversion of power system model. Energetic macroscopic representation (EMR) is used to model the power train of military vehicle[11].

Received : 30 August 2018, Revised : 25 February 2019
Accepted : 12 March 2019, Online published : 30 April 2019

Design of controllers is important for efficient energy management. Inputs to controller are derived from sensors and control actions are delivered to different actuators of the system. Sensors and Actuators called transducers play a major role in each control action. System includes transducers and other sub-systems, operating together to meet user specifications. Each subsystem is made of multiple electrical and electronics components having their own history regarding manufacturing and environmental conditions. The overall operation of the system depends on reliable functioning of the individual components. With the advancement in digital technology, these components can be made to carry their history in electronic form as defined by the IEEE 21450 standard[12-14] in the form of transducer electronic data sheet (TEDS). The TEDS are created for each transducer in the system. It is used to store the details of transducers like operating range, error, calibration details etc.

These TEDS can be accessed by TIM provided for the subsystems and the system as a whole depending on the level of modularity. A typical TIM architecture is as shown in Fig. 1.

2. SYSTEM MANAGEMENT

A supervisory digital management is provided to access the TIM and TEDS to enable the following levels of functions.

Level 1 : Access the Transducer data for appropriate calibration and identification of sensor/actuator failures and compensation for non-idealities. e.g. ADC offset error

Level 2 : Configure the TIM architecture to perform self calibration of sensors/actuators and embed the localised control of subsystems. The TIM architecture enables further global

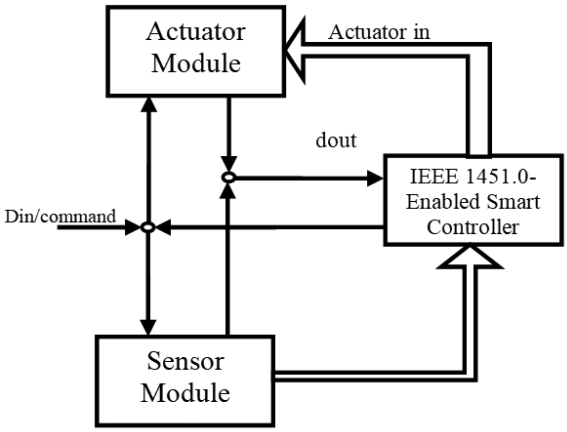

Figure 1. TIM-control architecture.

access of the calibrated data and the controller performance. e.g. Estimator based control algorithm to derive the optimum power generation from battery and engine.

Level 3 : Enables centralised performance optimisation through monitored data from TIM and TEDS. e.g. In-house battery status monitoring and redistribution of loads.

Block diagram representation of system management is as shown in Fig. 2. The architecture is designed for the power management of Series Hybrid Electric Vehicle with Diesel Engine, DC Motor and Battery. Actuator module consists of converter switches and controlled switches connected with engine, battery and load. Battery voltage/current, Motor voltage/current, speed and diesel engine output voltage/current are sensed by sensor module. Power derived from the engine and battery is controlled by solving linear quadratic regulator problem. IEEE21450 enabled controller is designed to execute smart transducer interface standard services and control algorithm in parallel.

The standard supports update of system modules and improves the system reliability using TEDS information. Proposed controller receives sensor data and executes IEEE21450 service commands in parallel. Level 1 function of the system is applied to the sensor data. Input sensor data is calibrated with the information provided by "Calibration TEDS". Calibration details include ADC offset error, sensor non-linearity, etc. Estimator based controller performs second level of system function. Speed of the vehicle and battery state of charge are considered as states of system. Power derived from engine and battery are chosen as control vectors. Third level of system function decides the switching pattern of loads based on the control vectors. Timing and control unit provides enable signal for all modules and appropriate clock signals according to the input /output devices. Synchronisation of different I/O devices with controller is achieved.

IEEE21450 Command generator and decoders unit decodes the commands in the instruction register through serial input called 'din'. Access/Update of TEDS, registers and transducers are executed through IEEE21450 service commands. Write operation of TEDS/Registers is performed through 'din' serial input. Similarly read operation is achieved with 'dout' serial output. TEDS is configured in the form of registers for fast access. Each transducer is implemented with three mandatory TEDS and one optional TEDS. Mandatory TEDS are Transducer Channel TEDS, User TEDS and Physical TEDS. Calibration details of transducers are stored in optional TEDS called "Calibration TEDS". TIM details are stored in "Meta TEDS" and it is mandatory TEDS. Total memory occupied by TEDS is 1668 for each sensor.

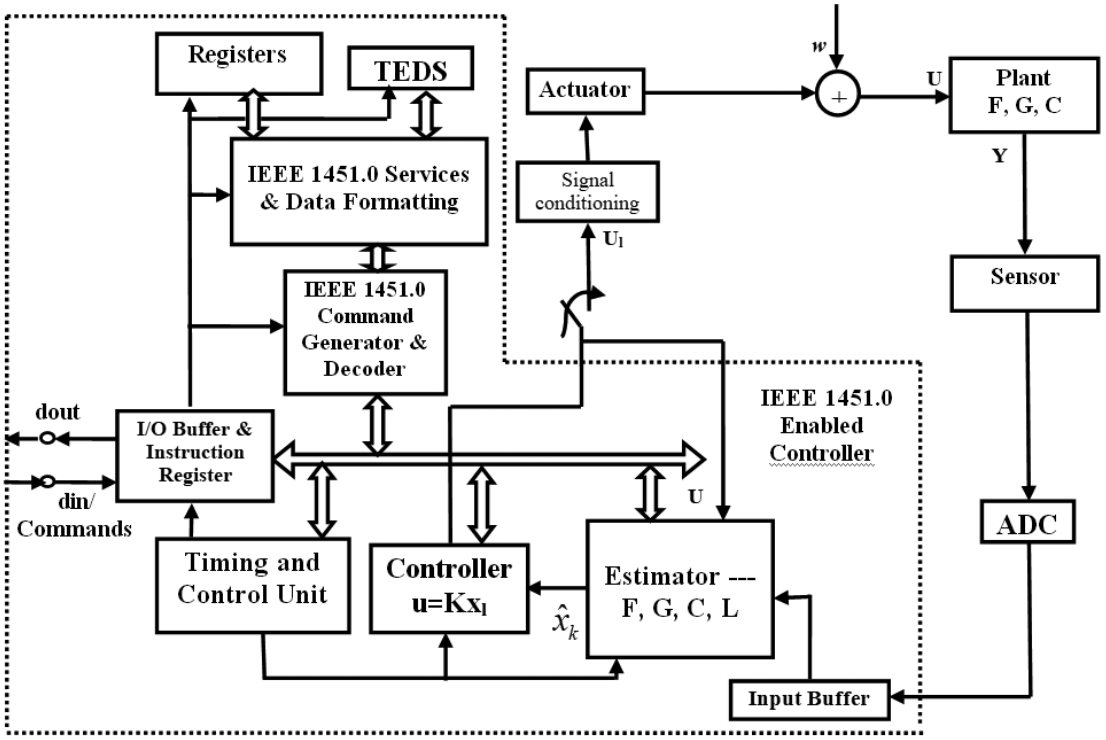

Figure 2. Block diagram representation of digital management.

3. SIMULATION RESULTS AND HARDWARE IMPLEMENTATION

Functionalities of the system are validated through simulation results provided by Xilinx tool. Calibaration of sensor data is as shown in Fig. 3. Input data received in the serial input is '3A' in hexadecimal form. Calibration data of '08' is subtracted and 32 is stored in the variable 'y'.

IEEE21450 service command to read 'User TEDS 1' is as shown in Fig. 5. Command is received in instruction register and contents of User TEDS is placed in 'dout' serial ouput.

Activation of estimator based controller is illustrated in Fig. 4. Sixteen bit architecure is chosen for estimator. It is simulated for the parameters F, G, and C as follows. The actuator signal is continuously generated by the control algorithm implemented in the FPGA

$$F = \begin{bmatrix} 0.983 & -0.1897 \\ 0.0948 & 0.895 \end{bmatrix} G = \begin{bmatrix} 0.1994 \\ 0.0097 \end{bmatrix} C = \begin{bmatrix} 0 & 1 \end{bmatrix}$$

Hardware implementation of the proposed architecture is discussed for two types of systems. First system is based on the series hybrid electric vehicle system for military vehicles described by Lu[10], *et al.* Battery state of charge and Vehicle speed are the parameters to be monitored to maintain in the desired values. Input parameters to be sensed are

- Battery voltage and current
- Engine output voltage and current
- Motor Voltage, current and speed
- Vehicle speed

A total of eight parameters are converted into digital signal by ADC0809. Digital data of 8-bits are processed by the smart controller. Eleven interface signals required in the input side are as follows.

- din – serial data input for IEEE21450 services (command and data)
- data – 8-bit data from ADC
- clk – clock 100MHz
- eoc – end of conversion from ADC

List of output signals provided by the controller are

- dout – serial data output for IEEE21450 services (status and data)
- ale – address latch enable to ADC
- sc – start conversion to ADC

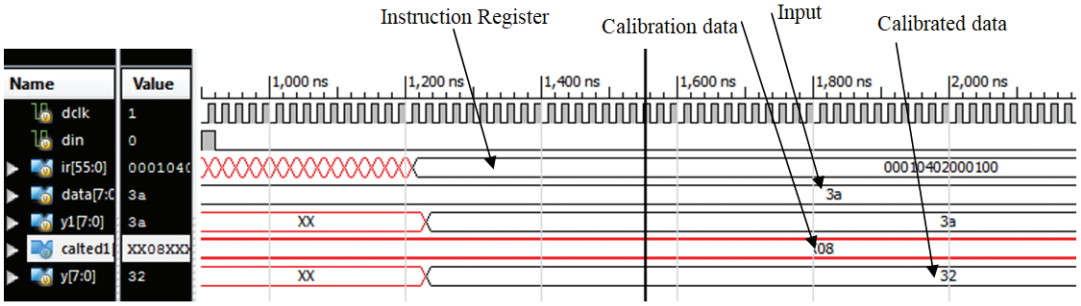

Figure 3. Calibration of sensor data.

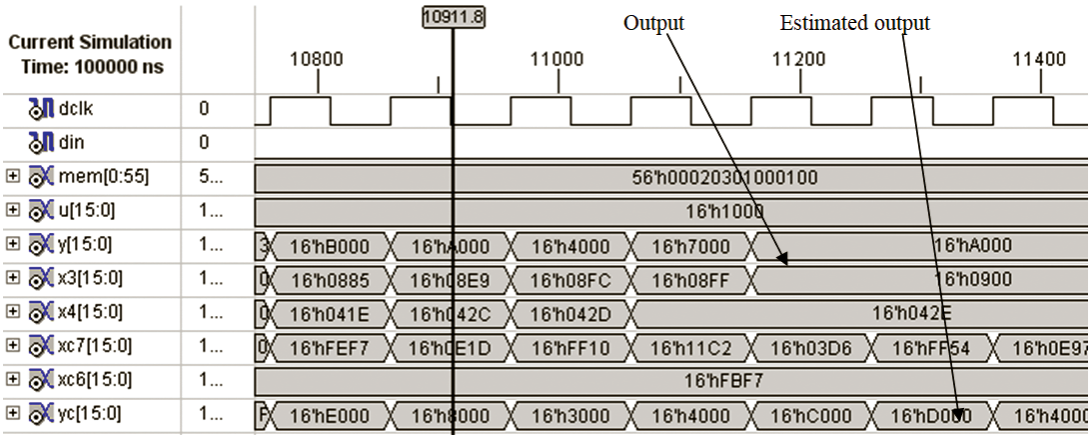

Figure 4. Estimator execution.

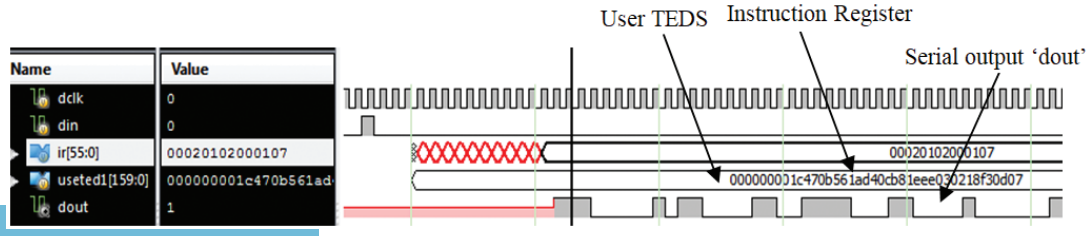

Figure 5. IEEE21450 Service command 'Read User TEDS'.

- add – 3 address lines to ADC
- adcclk – clock to ADC
- pwm1 – pwm signal for converter
- sw – 15 switch control signal to connect electrical loads to bus

This architecture is designed to process eleven input signals and generates twenty three output signals for optimum control. A total of thirty four input / output signals are used for interfacing. TEDS memory requirement is 10404 bits and 32 registers each of 8 bits are required. FPGA clock is fixed at 100 MHz, ADC clock at 500 kHz and converter switching frequency at 40 kHz.

Table 1. Synthesis report for smart controller

Device utilisation summary xc7a100t-3csg324			
Logic utilisation	**Used**	**Available**	**Utilisation (%)**
Number of slices	6812	126800	5
Number of slice flip flops	13433	63400	21
Number of 4 i/p LUTs	6771	13474	50
Number of input/output buffers	34	210	16

Timing summary:

Speed Grade: -3

Minimum period: 6.542 ns (Maximum Frequency: 152.851 MHz)

Minimum input arrival time before clock: 3.516 ns

Maximum output required time after clock: 0.746 ns

Maximum combinational path delay: No path found

Second architecture is designed for inversion based control of a highly redundant military hybrid electric vehicle[11]. It uses a total of 31 transducers for generation, storage and traction subsystem. Four numbers of ADC0809 are used to convert analog to digital signal. Each ADC is associated with 8-bit data output, one control input (eoc) and six outputs (add, ale, sc, adcclk). Fifteen I/O signal are required for single ADC and totally 60 I/O signals are required for input signal processing alone. In addition with this, 2 signals for IEEE21450 standard services, 1 clock signal and 16 switch control signals are required. The architecture is designed with 79 I/O signals. Hardware utilisation of this controller is increased four times that of previous architecture.

4. CONCLUSIONS

This architecture proposes knowledge based controller based on IEEE21450 standard. Implementation of the controller using FPGA enables fast and parallel control operations with ease of update of system modifications. More number of I/O pins supports parallel reception of inputs and simultaneous control of multiple output devices. It executes optimal control algorithm of power system and smart transducer interface standard services in parallel. Hardware utilisation report shows more functionalities could be included to enhance the system performance. Real time execution of system will be carried out by downloading the programming bit file into FPGA after implementation process.

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CONTRIBUTORS

Dr J. Kamala received her BE in Electronics and Communication Engineering from Madurai Kamaraj University in 1989, ME in VLSI Design from Bharathidasan University, in 2002 and PhD from Anna University in 2011. She is currently working as Associate Professor in the Department of Electronics and Communication Engineering, College of Engineering Guindy, Anna University, Chennai, India. Her research includes VLSI design, solar power, controller design and smart sensors.
In the current study, he discussed the structure of architecture with B. Umamaheswari and written the coding using Verilog for the proposed architecture.

Dr B. Umamaheswari received her BE (Electrical and Electronics Engineering) in 1985, ME (Power Systems Engineering) in 1988, and PhD in 1994 from Anna University and Postdoctoral Research in Application of Control theory from Faculty of Electrical Engineering, RMCS, Swindon, Cranfield University, UK (1995 - 1996). She is currently working as Professor in the Department of Electrical and Electronics Engineering, College of Engineering Guindy, Anna University, Chennai, India. Her research includes electrical machines, power systems, power electronics drives and control, modeling, analysis and control.
In the current study, he proposed the structure of the architecture in discussion with co-authors.

Mr T. Jaibalaganesh received his BE (Electronics and Communication Engineering) in 2008, ME (Applied Electronics) in 2010 from Anna University. He is currently pursuing the PhD at College of Engineering Guindy, Anna University, Chennai. His research includes VLSI implementation and PV system design.
In the current study, he did code development and simulation using Xilinx tool and implemented the architecture in a FPGA.